Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An electronic device including an authorization control circuit, comprising:

a data storage including one or more data files, wherein each of the data files is a digital audio file, video file, or multimedia file;

a digital signal processor operably coupled to the data storage, said digital signal processor operable (A) to provide digital data output, (B) to determine an authorization state by (a) receiving a data file selected by a user from the one or more data files, (b) hashing the data file to generate a fixed-length value or key representing the data file, and (c) comparing the fixed-length value or key to an expected fixed-length value or key for the data file, wherein the comparison determines if the data file has been changed or is an invalid copy, and ~~generating~~ (C) to generate a disable signal corresponding to the authorization state, wherein the disable signal is also capable of being generated when the electronic device satisfies one or more sleep conditions;

a digital to analog converter operably coupled to the digital signal processor and operable to receive the digital data output, convert the digital data to corresponding analog data, and output the ~~corresponding~~ analog data; ~~data, and mute the output of the corresponding analog data; and~~

the digital to analog converter including ~~an input~~ a mode input pin operable to receive the disable signal from the digital signal processor, and the digital to analog converter ~~muting the~~ operable to mute output of the ~~corresponding~~ analog data without adding noise artifacts in response to the disable ~~signal~~ signal;

wherein the digital signal processor has at least three output pins comprising a clock output pin to provide a clock signal, a mode output pin to provide the disable signal, and a digital data output pin to provide the digital data for conversion into analog data;

wherein the digital to analog converter further comprises a digital data input pin to receive the digital data for conversion, and a serial input pin to receive the clock signal to enable reception of the disable signal; and

wherein the digital to analog converter reads the state of the disable signal at the rising edges of the clock signal.

2. (Previously Presented) The electronic device of Claim 1, wherein the authorization state is either positive or negative and the digital signal processor is operable to generate the disable signal when the authorization state is negative.

3. (Cancelled)

4. (Currently Amended) The electronic device of Claim 1, wherein the digital to analog converter mutes the analog output ~~is muted~~ by filtering the received digital data prior to ~~conversion~~ converting the received digital data into analog data.

5. (Currently Amended) The electronic device of Claim 1, wherein the digital signal processor ~~further comprising: an output pin~~ is operable to transmit the disable signal as a high voltage on the mode output pin.

6. (Currently Amended) The electronic device of Claim 1, the digital to analog converter further comprising:

a pull-down circuit operable to create a low voltage at the input pin in the absence of a disable signal.

7-11. (Cancelled)

12. (Currently Amended) A method of selectively muting output in an electronic device, comprising the steps of:

generating digital data;

determining an authorization state, wherein determining the authorization state comprises:

~~selecting~~ retrieving a data file from one or more data files in a data storage device, wherein the data file is a digital audio file, video file, or multimedia file, said data file including the digital data, and wherein the retrieval is executed by a digital signal processor of the electronic device;

performing a hashing function on the data file to generate a fixed-length value or key representing the data file, wherein the hashing function is executed by [[a]] the digital signal processor; and

comparing the fixed-length value or key to an expected fixed-length value or key for the data file, wherein the comparison is executed by the digital signal processor to determine ~~determines~~ if the data file has been changed or is an invalid copy;

automatically generating a disable signal corresponding to the authorization state in response to a determination that the data file has been changed or is an invalid copy, wherein the disable signal is ~~also capable of being~~ generated by the digital signal processor and the digital signal processor is also operable to generate the disable signal when the electronic device satisfies one or more sleep conditions;

transmitting the digital data from the digital signal processor to a digital data input pin of a digital to analog converter;

generating, at the digital to analog converter, an analog signal corresponding to the digital data, and outputting the analog signal;

in response to a negative authorization state, automatically transmitting the disable signal from a mode output pin of the digital signal processor to a mode input pin of the digital to analog converter; ~~and~~

muting, at the digital to analog converter, the analog signal without adding noise artificats in response to receiving the ~~transmitted~~ disable signal at the digital to analog converter

receiving a clock signal from the digital signal processor at a serial input pin of the digital to analog converter; and

reading the state of the disable signal at the digital to analog converter at rising edges of the clock signal.

13. (Currently Amended) The method of Claim 12, wherein the step of muting comprises activating a digital filter in the digital to analog converter.

14-16. (Cancelled)

17. (Currently Amended) The method of ~~Claim 16~~ Claim 12, wherein the clock signal is transmitted to the digital to analog converter contemporaneously with the disable signal.

18. (Original) The method of Claim 12, further comprising the step of:

generating a power-save signal and wherein the disable signal is generated in response to the power-save signal.

19. (Previously Presented) The method of Claim 12, further comprising the steps of:

generating an override signal; and

terminating the muting step in response to the override signal.

20. (Previously Presented) The method of Claim 19, further comprising the step of:

detecting the step of generating the disable signal; and wherein the override signal is generated in response to the detection of the disable signal.

21. (Previously Presented) The circuit of Claim 1, wherein one of the sleep conditions is usage of the electronic device, said disable signal generated when the usage meets a predetermined criteria.

22. (Previously Presented) The circuit of Claim 1, wherein the electronic device is a music player, video player, or multimedia file player.

23. (Cancelled)

24. (New) The electronic device of Claim 1, wherein:

the electronic device further comprises a first signal line connecting the mode output pin of the digital signal processor directly to the mode input pin of the digital to analog converter, and a second signal line connecting the digital data output pin from the digital signal processor to the digital data input pin of the digital to analog converter;

the digital signal processor is operable to transmit mode data on the mode output pin, wherein the mode data comprises address bits, function bits, and a disable bit; and

the digital to analog converter is operable to read the disable bit within the mode data as the disable signal.

25. (New) The method of Claim 2, wherein the operation of reading the state of the disable signal at the digital to analog converter at rising edges of the clock signal comprises:

reading mode data from the digital signal processor at the mode input pin of the digital to analog converter, wherein the mode data comprises address bits, function bits, and a disable bit; and

at the digital to analog converter, reading the disable bit within the mode data as the disable signal.